UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,100	11/25/2003	Rainer Buchty	Buchty 1-7-1	9858

42292 7590 10/02/2006

LAW OFFICE OF JEFFREY M. WEINICK, LLC
615 WEST MT. PLEASANT AVENUE
LIVINGSTON, NJ 07039

EXAMINER	
TSAI, SHENG JEN	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 10/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/722,100	BUCHTY ET AL.	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicant's Remarks filed on August 29, 2006 regarding application 10,722,100 filed on November 25, 2003.

2. Claims 1-32 are pending for consideration.

3. ***Response to Remarks***

Applicants' remarks have been fully and carefully considered, with the Examiner's response set forth below.

Response to remarks on claim 1

Applicants contend that the prior art (Tanaka et al., US 4,910,667) does not disclose the VIR or the increment data itself being a vector; particularly, figure 1, item 13 of Tanaka et al. denote a group of vector increment registers but this group of vector increment registers is not disclosed as being a vector. Thus Tanaka et al. fails to teach the element of "an index vector comprising a plurality of values" as recited in claim 1. The Examiner disagrees with this assessment for the following reasons:

First, as Applicants agree, Tanaka et al. teach a group of registers each holding an increment value. Thus the teaching of the element of "a plurality of values" has been confirmed positively without any question.

Second, the issue of whether this "a plurality of values" is a "vector," or, more fundamentally, what constitutes a vector, is addressed. It is well understood, in science and engineering, that a vector is an entity that comprises multiple values/elements, as opposed to a scalar which is an entity that comprises a single value/element. The actual, physical implementation of a vector may take various different forms.

Third, figure 2, item 62 of Tanaka et al. provides further details regarding how the group of VI values is arranged. Note that they are in the form of "an index array," which is clearly in the form of a "vector," as one of ordinary skills in the art would agree. Figure 3, 109, 111 and 113 also illustrate that VI1, VI2 and VI3 being lined up in a "vector" form.

Thus the group of VI values disclosed by Tanaka et al. definitely qualifies as a vector.

Applicants also contend that the increment values VI1, VI2 and VI3 are not operated with the same starting based value, as required by claim 1. The Examiner disagrees with this assessment for the following reasons:

First, the wording of claim 1, as currently presented, states that "concurrently performing an operation on individual ones of said plurality of index vector values with a base value to generate a plurality of memory addresses." Note that it merely recites "a base value" in the general sense, but not "the same base value" as Applicants now contend.

Second, in the invention of Tanaka et al., each of the increment values VI1, VI2 and VI3 is added to a corresponding base value of VB1, VB2 or VB3, respectively, to generate a plurality of memory addresses. It is noted that the values of VB1, VB2 and VB3 may be the same or different. When their values are the same, it represents the case where "concurrently performing an operation on individual ones of said plurality of index vector values with the same base value to generate a plurality of memory addresses."

Thus this element recited in claim 1 is also clearly taught by Tanaka et al.

Therefore, the Examiner's position regarding the status of claim 1, and those claims dependent from it, remains the same as stated in the previous Office Action.

Response to remarks on claim 19

Applicants again contend that the group of VI values is not a vector. This issue has been fully addressed earlier in this Office Action. Refer to "Response to remarks on claim 1" for details.

Applicants further contend that Tanaka et al. do not teach the element of "a plurality of operator circuits" as recited in claim 19, due to the use of separate start addresses VB1, VB2 and VB3. This issue also has been fully addressed earlier in this Office Action. Refer to "Response to remarks on claim 1" for details.

Thus, Applicants' remarks on claim 19 are not valid considering the explanation provided in "Response to remarks on claim 1," and the Examiner's position regarding the status of claim 19, and those claims dependent from it, remains the same as stated in the previous Office Action.

Response to remarks on claims 7 and 25

Applicants contend that, in the invention of Tanaka et al., each memory address is not accessed using a corresponding memory, but instead in the main storage. The Examiner disagrees with this assessment for the following reasons:

First, it was explained in the previous Office Action that "the corresponding a plurality of memory units including the main storage (figure 3, 96) and the vector buffer

storage (figure 3, 21); figure 5 further shows the case where a plurality of vector buffer storages (221-1 and 221-2) are present."

Second, it was further explained in the previous Office Action that "If the vector buffer storage control 20 determines that the desired vector data is in the vector buffer storage 21, it sends the address of the vector data and a read signal to the vector buffer storage 21 through a line l41, and sends a select signal through a line l39 so that the vector data is transferred from the vector buffer storage 21 to the vector registers 98 through the selector 71." Thus the memory address is clearly used to access the corresponding memory unit, which in this case is the vector buffer storage and not the main storage.

Applicants further contend that, regarding claim 25, Tanaka et al. do not teach the element of "wherein individual ones of said plurality of memory units is coupled to an output of a corresponding operator circuit" because figures 3 and 5 of Tanaka et al. show that the output of all of the requestors is coupled to the main storage. The Examiner disagrees with this assessment for the following reason:

Figure 3 Tanaka et al. clearly shows that the outputs of the requestors (IO3, IO4 and IO5) are coupled to the vector buffer storage via connections (I141, I142 and I143) through the storage control.

Therefore, the Examiner's position regarding the status of claims 7 and 25 remains the same as stated in the previous Office Action.

Response to remarks on claims 10 and 26

Applicants traverse the rejections on claims 10 and 26 based on the argument that Tanaka et al. do not teach "concurrently generating memory addresses using a plurality of values from an index vector with the same base value."

However, it has already been established earlier in this Office Action that Tanaka et al. indeed disclose this limitation (refer to "Response to remarks on claim 1" for details). Thus Applicants' traversals are not valid.

Therefore, the Examiner's position regarding the status of claims 10 and 26 remains the same as stated in the previous Office Action.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-2, 7-9, 19-20, 25 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka et al. (US 4,910,667).

As to claim 1, Tanaka et al. disclose **a method** [Vector Processor with Vector Buffer Memory for Read or Write of Vector Data between Vector Storage and Operation Unit (title)] **for accessing at least one memory unit** [the corresponding memory unit including the main storage (figure 3, 96) and the vector buffer storage (figure 3, 21); figure 5 further shows the case where a plurality of vector buffer storages (221-1 and 221-2) are present] **based on an index vector comprising a plurality of values** [the corresponding index vector comprising Vector Base Registers (VB1, VB2

and VB3, figure 1, 12; figure 3, 108, 110 and 112), Vector Increment Registers (VI1, VI2 and VI3, figure 1, 13; figure 3, 109, 111 and 113), and Vector Length Registers (VL1, VL2 and VL3, figure 1, 11; figure 3, 11); refer to "Response to remarks on claim 1" presented earlier in this Office Action], **said method comprising the steps of**: **concurrently performing an operation on individual ones of said plurality of index vector values with a base value to generate a plurality of memory addresses** [refer to "Response to remarks on claim 1" presented earlier in this Office Action; The content of the vector base register VBR selected from the group of registers 12 by the field R2 14-3 is sent to the vector buffer storage control 20, the fetch requestor 94 and the store requestor 95 through a line l31. It indicates the start address of the vector data in the main storage. The content of the vector increment register VIR selected from the group of registers 13 by the field R3 14-4 is sent to the vector buffer storage control 20, the fetch requestor 94 and the store requestor 95 through a line l32. It indicates the increment for the vector data. The start address and the increment are keys to check whether the necessary vector data is stored in the vector buffer storage 21. In the present identification embodiment, the start address and the increment are used as the information to identify the vector data (column 4, lines 26-42); Note that 3 requestors (figure 3, 103, 104 and 105) are present to support concurrent operations of the 3 sets of Vector Base Registers and Vector Increment Registers]; **and**

concurrently accessing individual ones of said plurality of memory addresses in said at least one memory unit [Note that 3 requestors (figure 3, 103, 104 and 105)

are present to support concurrent accessing of the 3 memory locations specified by the 3 sets of Vector Base Registers and Vector Increment Registers; the location of the vector data on the main storage 96 is designated by 108 and 113. The address of the two vector data to be read are designated by VB1 108, VI1 109, VB2 110 and VI2 111, where VB represents a start address of the vector data and VI represents an increment for the vector data. The address on the main storage of the vector data to be stored is designated by VB3 112 and VI3 113. The VB1 and VI1 are sent to the vector buffer storage control 102 and the fetch requestor 103. The VB2 and VI2 are sent to the vector buffer storage control 102 and the fetch requestor 104. The VB3 and VI3 are sent to the vector buffer storage control 103 and the store requestor 105 (column 7, lines 40-53)].

As to claim 2, Tanaka et al. teach that **said operation is addition** [The content of the vector base register VBR selected from the group of registers 12 by the field R2 14-3 is sent to the vector buffer storage control 20, the fetch requestor 94 and the store requestor 95 through a line l31. It indicates the start address of the vector data in the main storage. The content of the vector increment register VIR selected from the group of registers 13 by the field R3 14-4 is sent to the vector buffer storage control 20, the fetch requestor 94 and the store requestor 95 through a line l32. It indicates the increment for the vector data. The start address and the increment are keys to check whether the necessary vector data is stored in the vector buffer storage 21. In the present identification embodiment, the start address and the increment are used as the

information to identify the vector data (column 4, lines 26-42). Note that "increment" means "addition"].

As to claim 7, Tanaka et al. teach that **at least one memory unit comprises a plurality of memory units** [the corresponding memory unit including the main storage (figure 3, 96) and the vector buffer storage (figure 3, 21); figure 5 further shows the case where a plurality of vector buffer storages (221-1 and 221-2) are present] **and wherein said step of concurrently accessing comprises the step of accessing individual ones of said plurality of memory addresses in one corresponding memory unit** [refer to "Response to remarks on claims 7 and 25" presented earlier in this Office Action; If the vector buffer storage control 20 determines that the desired vector data is in the vector buffer storage 21, it sends the address of the vector data and a read signal to the vector buffer storage 21 through a line l41, and sends a select signal through a line l39 so that the vector data is transferred from the vector buffer storage 21 to the vector registers 98 through the selector 71. If the vector buffer storage control 20 determines that the desired vector data is not in the vector buffer storage 21, it activates the fetch requestor 94 through a line l43 to send the vector data to the vector registers 98 from the main storage 96 through the storage control 97, a line l38 and the selector 71. The address of the vector data and a write signal are sent from the vector buffer storage control 20 through a line l42, and the vector data is written into the vector buffer storage 21 through a line l38 (column 4, lines 43-59)].

As to claim 8, Tanaka et al. teach that **the step of concurrently accessing further comprises the steps of:**

concurrently reading data [Read Control, figure 2, 68)] **from individual ones of said plurality of memory addresses** [Note that 3 requestors (figure 3, 103, 104 and 105) are present to support concurrent accessing of the 3 memory locations specified by the 3 sets of Vector Base Registers and Vector Increment Registers; the location of the vector data on the main storage 96 is designated by 108 and 113. The address of the two vector data to be read are designated by VB1 108, VI1 109, VB2 110 and VI2 111, where VB represents a start address of the vector data and VI represents an increment for the vector data. The address on the main storage of the vector data to be stored is designated by VB3 112 and VI3 113. The VB1 and VI1 are sent to the vector buffer storage control 102 and the fetch requestor 103. The VB2 and VI2 are sent to the vector buffer storage control 102 and the fetch requestor 104. The VB3 and VI3 are sent to the vector buffer storage control 103 and the store requestor 105 (column 7, lines 40-53)]; **and**

storing said data in a storage register [the corresponding storage register is the vector registers (figure 1, 98)]

As to claim 9, Tanaka et al. teach that **the step of concurrently accessing further comprises the step of concurrently writing data to individual ones of said plurality of memory addresses** [Write Control, figure 2, 69; Note that 3 requestors (figure 3, 103, 104 and 105) are present to support concurrent accessing of the 3 memory locations specified by the 3 sets of Vector Base Registers and Vector Increment Registers; the location of the vector data on the main storage 96 is designated by 108 and 113. The address of the two vector data to be read are

designated by VB1 108, VI1 109, VB2 110 and VI2 111, where VB represents a start address of the vector data and VI represents an increment for the vector data. The address on the main storage of the vector data to be stored is designated by VB3 112 and VI3 113. The VB1 and VI1 are sent to the vector buffer storage control 102 and the fetch requestor 103. The VB2 and VI2 are sent to the vector buffer storage control 102 and the fetch requestor 104. The VB3 and VI3 are sent to the vector buffer storage control 103 and the store requestor 105 (column 7, lines 40-53)].

As to claim 19, Tanaka et al. disclose **an apparatus** [figures 1-6] **comprising**:

a first storage register for storing an index vector comprising a plurality of values [Vector Increment Registers (VI1, VI2 and VI3, figure 1, 13; figure 3, 109, 111 and 113)];

a second storage register for storing a base value [Vector Increment Registers (VI1, VI2 and VI3, figure 1, 13; figure 3, 109, 111 and 113)];

a plurality of operator circuits [3 requestors (figure 3, 103, 104 and 105) are present to support concurrent accessing of the 3 memory locations specified by the 3 sets of Vector Base Registers and Vector Increment Registers], **individual ones of said plurality of operator circuits having a first input coupled to at least a portion of said first storage register and a second input coupled to said second storage register, said plurality of operator circuits for performing an operation on individual ones of said index vector values with said base value to generate a plurality of memory addresses on outputs of said operator circuits** [refer to "Response to remarks on claim 19" presented earlier in this Office Action; figures 3-6;

the location of the vector data on the main storage 96 is designated by 108 and 113. The address of the two vector data to be read are designated by VB1 108, VI1 109, VB2 110 and VI2 111, where VB represents a start address of the vector data and VI represents an increment for the vector data. The address on the main storage of the vector data to be stored is designated by VB3 112 and VI3 113. The VB1 and VI1 are sent to the vector buffer storage control 102 and the fetch requestor 103. The VB2 and VI2 are sent to the vector buffer storage control 102 and the fetch requestor 104. The VB3 and VI3 are sent to the vector buffer storage control 103 and the store requestor 105 (column 7, lines 40-53)]; **and**

at least one memory unit [the corresponding memory unit including the main storage (figure 3, 96) and the vector buffer storage (figure 3, 21)] **coupled to the outputs of said operator circuits such that said plurality of memory addresses are accessible in said at least one memory unit** [figure 3; If the vector buffer storage control 20 determines that the desired vector data is in the vector buffer storage 21, it sends the address of the vector data and a read signal to the vector buffer storage 21 through a line l41, and sends a select signal through a line l39 so that the vector data is transferred from the vector buffer storage 21 to the vector registers 98 through the selector 71. If the vector buffer storage control 20 determines that the desired vector data is not in the vector buffer storage 21, it activates the fetch requestor 94 through a line l43 to send the vector data to the vector registers 98 from the main storage 96 through the storage control 97, a line l38 and the selector 71. The address of the vector data and a write signal are sent from the vector buffer storage control 20

through a line l42, and the vector data is written into the vector buffer storage 21 through a line l38 (column 4, lines 43-59)].

As to claim 20, refer to "As to claim 1" presented earlier in this Office Action.

As to claim 25, refer to "As to claim 7" presented earlier in this Office Action.

As to claim 32, refer to "As to claim 7" presented earlier in this Office Action.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US 4,910,667), and in view of Matsugami et al. (US 5,929,928).

As to claims 3 and 21, Tanaka et al. do not teach that said operation is bit replacement.

However, Matsugami et al. teach in their invention "Digital Image Processor" a method and apparatus of accessing image memory [figure 6] where a "Bit Replacement Circuit" [figure 11, 54] is used [column 9, lines 21-60].

The use of a bit replacement circuit allows the direct substitution of all or portion of a bit pattern to generate a new bit pattern, and is usually faster than other operations such as addition or Boolean operations [column 9, lines 21-60].

Therefore, it would have been obvious for one of ordinary skills at the time of Applicants' invention to recognize the benefits of using a bit replacement circuit, as

demonstrated by Matsugami et al., and to incorporate it into the existing apparatus disclosed by Tanaka et al. to further improve the performance of the system.

8. Claims 3-5, 14-16, and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US 4,910,667), and in view of Lavelle et al. (US 5,649,142).

As to claims 3-5, 14-16 and 21-23, Tanaka et al. do not teach **the bit replacement operations as recited in the claims**.

However, Lavelle et al. teach in their invention "Method and Apparatus for Translating Addresses Using Mask and Replacement Value Registers and for Accessing a Service Routine in Response to a Page Fault" a method and apparatus of translating a first address in a first address space to a second address in a second address space [abstract; figure 4] where a "Bit Replacement Circuit" [figure 4, 406, 408, 412, 414, 418, 420 and 422] including a "0-20 bit replacement value" [figure 4, 418] is used to replace the least significant bits [bits 0-20] of a 32-bit virtual address [figure 4, 402] to generate a 32-bit physical address [figure 4, 422]. Note the inclusion of the "compare address for page match determination" unit [figure 4, 414], which facilitates the detection of a particular address pattern, such as all 0's, that would be present in bits 0-20. Also note that the 32-bit address is formed by concatenating bits 0-20 [figure 4, 418] and bits 21-32 [bit offset, figure 4, 420].

The use of a bit replacement circuit is vital in supporting single-instruction, multiple-data (SIMD) architecture in which multiple processor units executing the same

instruction on a plurality of data, as the addresses of the plurality of data must be generated efficiently [column 1, lines 21-67].

Therefore, it would have been obvious for one of ordinary skills at the time of Applicants' invention to recognize the benefits of using a bit replacement circuit in support of a SIMD environment, as demonstrated by Lavelle et al., and to incorporate it into the existing apparatus disclosed by Tanaka et al. to further improve the performance of the system.

9. Claims 6, 17, 24 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US 4,910,667), and in view of Gurney et al. (US 6,745,315).

As to claims 6, 17, 24 and 31, Tanaka et al. do not teach that **the memory unit comprises a multiport memory unit**.

However, Gurney et al. teach in their invention "Generation of Address Pattern through Employment of One or More Parameters to Store Information at Parts of Storage That Are Employable with Multiprocessor" a method and apparatus of generating address pattern [abstract; figures 2-3] where a plurality of dual port memory units are employed [figure 3, 760] from which vector data is generated [figures 8 and 10].

The use of multiport memory units allows the simultaneous accessing via the two ports by two processors, hence increasing the throughput of the system.

Therefore, it would have been obvious for one of ordinary skills at the time of Applicants' invention to recognize the benefits of using multiport memory units in

support of a multi-processor environment, as demonstrated by Gurney et al., and to incorporate it into the existing apparatus disclosed by Tanaka et al. to further improve the throughput of the system.

10. Claims 10-13, 18, and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US 4,910,667), and in view of Shahidzadeh et al. (US 6,349,380).

As to claim 10, Tanaka et al. disclose **a method for accessing at least one memory unit based on an index vector comprising a plurality of segments** [refer to "As to claim 1" presented earlier in this Office Action], **said method comprising the steps of**:

concurrently performing an operation on a value stored in individual ones of said index vector segments with a base value to generate a first plurality of memory addresses [refer to "As to claim 1" presented earlier in this Office Action; refer to "Response to remarks on claim 10 and 26" presented earlier in this Office Action];

Regarding claim 10, Tanaka et al. do not teach **adding said base value to a value represented by the concatenation of said plurality of segments of said index vector to generate a single memory address; and**

concurrently accessing in said at least one memory unit either said first plurality of memory addresses or said single memory address.

However, Shahidzadeh et al. teach in their invention "Linear Address Extension and mapping to Physical memory using 4 and 8 Byte page Table Entries in a 32-bit

Microprocessor" a method and apparatus of generating address by concatenating the values from two registers [abstract; figure 9; figure 10] wherein **adding said base value** [the offset value, figure 9, 910 is added to a value from a segment descriptor which comprises two segments: Segment Selector (904) and Segment Extension (914)] **to a value represented by the concatenation of said plurality of segments of said index vector to generate a single memory address** [the offset value, figure 9, 910 is added to a value from a segment descriptor which comprises two segments: Segment Selector (904) and Segment Extension (914)]; **and concurrently accessing in said at least one memory unit either said first plurality of memory addresses or said single memory address** [figures 10 and 10A show the choice of the two possible address sources].

The use of such a memory addressing scheme allows the increase of linear address space of a microprocessor, which in turn provides larger user and system space and reduces the burden associated with linear address exhaustion for a larger physical address space [column 5, lines 12-15].

Therefore, it would have been obvious for one of ordinary skills at the time of Applicants' invention to recognize the benefits of using such a memory addressing scheme, as demonstrated by Shahidzadeh et al., and to incorporate it into the existing apparatus disclosed by Tanaka et al. to further improve the performance of the system.

As to claim 11, Shahidzadeh et al. teach that **whether said first plurality of memory addresses or said single memory address is accessed is based on a mode select signal** [Some IA-32 microprocessors employ several modes for

translating linear addresses into physical addresses, and we shall consider three such modes herein referred to as modes A, B, and C. Mode A supports a 32 bit physical address space with 4 KB page sizes. Mode B supports a 32 bit physical address space with either 4 KB or 4 MB page sizes. For modes A and B, the page and directory table entries are each 4 bytes. Mode C supports a 36 bit physical address space for a physical address size of 64 GB (physical address extension) with either 4 KB or 2 MB page sizes. For mode C, the page and directory table entries are each 8 bytes. For each mode, the page and directory tables are equal in size to a page. All modes are for translating 32 bit linear addresses (column 4, lines 16-28)].

As to claim 12, Shahidzadeh et al. teach that **mode select signal is programmable** [Some IA-32 microprocessors employ several modes for translating linear addresses into physical addresses, and we shall consider three such modes herein referred to as modes A, B, and C. Mode A supports a 32 bit physical address space with 4 KB page sizes. Mode B supports a 32 bit physical address space with either 4 KB or 4 MB page sizes. For modes A and B, the page and directory table entries are each 4 bytes. Mode C supports a 36 bit physical address space for a physical address size of 64 GB (physical address extension) with either 4 KB or 2 MB page sizes. For mode C, the page and directory table entries are each 8 bytes. For each mode, the page and directory tables are equal in size to a page. All modes are for translating 32 bit linear addresses (column 4, lines 16-28)].

As to claim 13, refer to "As to claim 2" presented earlier in this Office Action.

As to claim 18, refer to "As to claim 7" presented earlier in this Office Action.

As to claim 26, refer to "As to claim 1" and "As to claim 10" presented earlier in this Office Action.

As to claim 27, refer to "As to claim 2" presented earlier in this Office Action.

11. Claims 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US 4,910,667), in view of Shahidzadeh et al. (US 6,349,380), and further in view of Lavelle et al. (US 5,649,142).

As to claims 28-30, neither Tanaka et al. nor Shahidzadeh et al. teach **the bit replacement operations as recited in the claims**.

However, Lavelle et al. teach in their invention "Method and Apparatus for Translating Addresses Using Mask and Replacement Value Registers and for Accessing a Service Routine in Response to a Page Fault" a method and apparatus of translating a first address in a first address space to a second address in a second address space [abstract; figure 4] where a "Bit Replacement Circuit" [figure 4, 406, 408, 412, 414, 418, 420 and 422] including a "0-20 bit replacement value" [figure 4, 418] is used to replace the least significant bits [bits 0-20] of a 32-bit virtual address [figure 4, 402] to generate a 32-bit physical address [figure 4, 422]. Note the inclusion of the "compare address for page match determination" unit [figure 4, 414], which facilitates the detection of a particular address pattern, such as all 0's, that would be present in bits 0-20. Also note that the 32-bit address is formed by concatenating bits 0-20 [figure 4, 418] and bits 21-32 [bit offset, figure 4, 420].

The use of a bit replacement circuit is vital in supporting single-instruction, multiple-data (SIMD) architecture in which multiple processor units executing the same

instruction on a plurality of data, as the addresses of the plurality of data must be generated efficiently [column 1, lines 21-67].

Therefore, it would have been obvious for one of ordinary skills at the time of Applicants' invention to recognize the benefits of using a bit replacement circuit in support of a SIMD environment, as demonstrated by Lavelle et al., and to incorporate it into the existing apparatus disclosed by Tanaka et al. to further improve the performance of the system.

12. Claims 17 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US 4,910,667), in view of Shahidzadeh et al. (US 6,349,380), and further in view of Gurney et al. (US 6,745,315).

As to claims 17 and 31, neither Tanaka et al. nor Shahidzadeh et al. teach that **the memory unit comprises a multiport memory unit**.

However, Gurney et al. teach in their invention "Generation of Address Pattern through Employment of One or More Parameters to Store Information at Parts of Storage That Are Employable with Multiprocessor" a method and apparatus of generating address pattern [abstract; figures 2-3] where a plurality of dual port memory units are employed [figure 3, 760] from which vector data is generated [figures 8 and 10].

The use of multiport memory units allows the simultaneous accessing via the two ports by two processors, hence increasing the throughput of the system.

Therefore, it would have been obvious for one of ordinary skills at the time of Applicants' invention to recognize the benefits of using multiport memory units in

support of a multi-processor environment, as demonstrated by Gurney et al., and to incorporate it into the existing apparatus disclosed by Tanaka et al. and Shahidzadeh et al. to further improve the throughput of the system.

13. ***Related Prior Art of Record***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Kashiyama et al., (US 5,247,695), "Vector Processor with Byte Access of Memory."
- Omoda et al., (US 4,677,547), "Vector Processor."
- Takamine et al., (US 4,811,213), "Vector Processor with Vector Registers."
- Aoyama et al., (US 4,991,083), "Method and system for extending Address Space for Vector Processing."
- Kinoshita, (US 5,887,182), "Multiprocessor System with Vector Pipelines."
- Cray, Jr., (US 4,128,880), "Computer Vector Register Processing."
- Yokoyama, (US 5,136,699), "Logical Address Generating Device for an Instruction Specifying Two Words, each Divided into Two Parts."
- Fujii et al., (US 5,437,043), "Information Processing Apparatus Having a Register File Used Interchangeable Both as Scalar Registers of Register Windows and as vector Registers."
- Mishina et al., (US 5,010,483), "Vector Processor Capable of Indirect Addressing."

- Omoda et al., (US 4,825,361), "Vector Processor for Reordering Vector Data During Transfer from Main Memory to Vector Registers."
- Potash et al., (US 4,760,518), "Bi-Directional Databus System for Supporting Superposition of Vector and Scalar Operations in a Computer."

Conclusion

14. Claims 1-32 are rejected as explained above.

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

September 15, 2006

PIERRE BATAILLE
PRIMARY EXAMINER
9/26/06